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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/652,327	08/29/2003	Uri Elzur	13945US02	1636

23446 7590 09/24/2007

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EXAMINER	
HOANG, HIEU T	

ART UNIT	PAPER NUMBER
2152	

MAIL DATE	DELIVERY MODE
09/24/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/652,327	ELZUR ET AL.	
	Examiner	Art Unit	
	Hieu T. Hoang	2152	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 September 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08/29/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the communication filed on 09/07/2007.

2. Claims 1-28 are pending and presented for examination.

Response to Arguments

3. Applicant's arguments have been fully considered but they are not persuasive.

4. Argument one is on page 10 of the Remarks wherein the applicant argues that the prior art does not teach: "a network connector; a processor coupled to the network connector". The examiner respectfully traverses the argument. Boucher in fig. 13 and col. 16 lines 6-10 shows four network lines for the purpose of supporting different conduits (such as twisted pair, coaxial cable or optical fiber), not for supporting each traffic on a different connector. Furthermore, there is no need for Boucher's network interface card to have four network connectors for it to function. If one conduit is used alone, the connector is fully capable of communicating a plurality of network traffics as indicated in the second limitation of claim 1.

5. Argument two is on page 11 wherein the applicant argues that the prior art does not teach: "a unified driver coupled to the PCI bridge." The examiner respectfully traverses. Claim 1 recites a unified driver coupled to the PCI bridge, given broadest reasonable interpretation, meaning the device driver is somewhat connected to the PCI bridge either directly or indirectly. A device driver is a software entity and a PCI bridge is a hardware entity, so they can only be connected conceptually and not physically. A device driver works in Kernel domain while the PCI bridge works in hardware domain.

Boucher in fig. 6, col. 9 lines 20-35, and fig. 11 shows clearly shows a PCI bridge 157 coupled to the software protocol stack (same stack in figs. 6 and 11) that has an INIC driver, and inherently they have to be connected as suggested in fig. 6.

6. Argument three on claim 18 is on page 13 wherein the applicant argues that the prior art does not teach: "a layer 2 connector." The examiner respectfully traverses. As discussed in argument 1, Boucher's each connector is capable of transporting a plurality of network traffics, and there is no absolute need for Boucher to have 4 connectors for the INIC to function, since each connector supports a different conduit, not traffic.

7. Argument four is on page 14 wherein the applicant argues that the prior art does not teach: "a single data path." The examiner respectfully traverses. Referring to fig. 2 of the specification, the single path in the application is a single line connecting hardware entities above PCI bridge 440 and software driver 450. Boucher's fig. 10 shows a single path between the hardware INIC and the INIC miniport driver, absolutely reading on the claimed single path. The two paths that the applicant mentioned in the argument are actually two paths split by INIC miniport driver 306 between components 306 and 202 so that data can be processed by the fast stack or the conventional slow stack depending on a label on the data (Boucher, col. 14 lines 8-12). It is further submitted that these two paths are not same as the one disclosed in the specification, they are more similar to the paths between driver 450 and components such as 460, 470, 510, 520 in fig. 2 of the application. So arguments regarding these paths are moot.

8. Any later arguments involving "a network connector; a processor coupled to the network connector" and "a unified driver coupled to the PCI bridge" is moot for the rationale given above.

9. Argument five is on page 18 wherein the applicant argues that the prior art does not teach: "a unified driver is coupled to a software TCP processor and to a socket service switch." The examiner respectfully traverses. Referring to fig. 2 of the specification, the components claimed are driver 450, TCP socket processor 460 and socket service switch 470. This arrangement is completely analogous to fig. 1 of Microsoft, wherein a NDIS driver is coupled to a TCP/IP/Sockets provider and then a socket service switch.

10. On pages 19-22, the applicant traversed the Official Notice taken that "employ time division multiplexing (TDM) to transmit multiple traffics over one channel in different timeslots" and "dynamically allocating fixed resources between among the different types of network traffic". In response, the examiner submits that the Microsoft Computer Dictionary (fifth edition) defines TDM as a form of multiplexing in which transmission time is broken into segments, each of which carries one segment of one signal, reading on "time division multiplexing (TDM) to transmit multiple traffics over one channel in different timeslots." "Dynamically allocating fixed resources between among the different types of network traffic", given its broadest interpretation, means dynamically allotting amount of resource(s) for each type of traffic, which is known to one skilled in the art how to implement (see Yang et al. US 2002/0041566, abstract).

11. Argument six is on page 23 wherein the applicant argues that the prior art Boucher–Hayes does not disclose an "upper layer processor." Hayes in [0017] discloses an offloading iSCSI over TCP/IP processor residing on a NIC. iSCSI is an upper layer protocol, so the iSCSI processor is analogous to applicant's processor 500 for processing iSCSI traffic in fig. 2.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

13. Claims 1-4, 15-20, and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Boucher et al. (US 6,226,680, hereafter Boucher).

14. For claim 1, Boucher discloses a server, comprising:

- a network connector (fig. 13, col. 16 lines 6-12, network line 210, four network lines are presented for different conduits, but each of them is a media independent interface);

- a processor coupled to the network connector (fig. 13, microprocessor 470, col. 16 line 62-col. 17 line 13), the processor being operable to process a plurality of different types of network traffic (abstract, col. 3 lines 35-67, col. 13 lines 24-35, the intelligent network interface card INIC's processor supports an offload traffic via fast path and regular IP traffic via a slow path);
- a peripheral component interface (PCI) bridge coupled to the processor (fig. 13, PIC bus interface unit); and
- a unified driver coupled to the PCI bridge, the unified driver being operable to provide drivers associated with the plurality of different types of network traffic (fig. 6 and 10, PCI bridge 157 connected to protocol stack with driver, col. 14 l. 9-13 and 61-66, INIC miniport driver determines whether the traffic is fast path offload traffic and slow path IP traffic).

15. For claim 2, Boucher further discloses the network connector comprises an Ethernet connector (fig. 13, network line 210 is an Ethernet connector).

16. For claim 3, Boucher further discloses the plurality of different types of network traffic comprises at least two of common Ethernet traffic, offload traffic, storage traffic and remote direct memory access (RDMA) traffic (same rationale as in claim 1, Ethernet traffic and offload traffic).

17. For claim 4, Boucher further discloses the processor comprises a single integrated chip (fig. 9, fig. 13, microprocessor).

18. For claim 15, Boucher further discloses the processor or the PCI bridge determines which of the different types of network traffic accesses a particular service provided by the server (fig. 10 and 11, col. 14 l. 9-13 and 61-66, INIC miniport driver determines whether the traffic is fast path offload traffic and slow path IP traffic).

19. For claim 16, the claim is rejected for the same rationale as in claim 13.

20. For claim 17, Boucher further discloses the processor, the PCI bridge or the unified driver provides a unified data and control path (fig. 10 and 11, col. 14 l. 9-13 and 61-66, INIC miniport driver determines whether the traffic is fast path offload traffic and slow path IP traffic).

21. For claim 18, Boucher discloses a method for network interfacing, comprising:
(a) handling a plurality of different types of network traffic via a layer 2 (L2) connector (fig. 13, col. 16 lines 6-12, a network line 210 connected to a MAC controller supporting both offload traffic and regular IP traffic);
(b) processing the different types of network traffic in a single chip (fig. 13, microprocessor 470, col. 16 line 62-col. 17 line 13, col. 3 lines 35-67, the INIC supports an offload traffic via fast path and regular IP traffic via a slow path); and

(c) determining which of the different types of network traffic accesses software services via a single data path (fig. 10 and 11, col. 14 l. 9-13 and 61-66, INIC miniport driver determines whether the traffic is fast path offload traffic and slow path IP traffic, single line connecting INIC and INIC miniport driver).

22. For claim 19, Boucher further discloses the plurality of different types of network traffic comprises at least two of common Ethernet traffic, offload traffic, storage traffic, interprocess communication (IPC) traffic and management traffic (same as claim 3).

23. For claim 20, Boucher further discloses the L2 connector is a single L2 connector (fig. 13, col. 16 lines 6-12, a network line 210 connected to a MAC controller, four network lines are presented for different conduits, but each of them is media independent interface).

24. For claim 23, Boucher further discloses: (a) providing drivers associated with the plurality of different types of network traffic via a unified driver (fig. 11 INIC miniport driver for both offload traffic and regular IP traffic).

Claim Rejections - 35 USC § 103

25. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

26. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boucher, as applied to claim 1 above, and further in view of Kistler et al. (US 2002/0198934, hereafter Kistler)

27. For claims 10 and 11, Boucher discloses the invention as in claim 1. Boucher does not disclose a server management agent coupled to the processor that is coupled to a keyboard and/or video and/or mouse service.

However, Kistler discloses the same (fig. 3 keyboard and mouse connected to an emulator that is coupled to a NIC)

Therefore, it would have been obvious for one skilled in the art at the time of the invention to combine the teachings of Boucher and Kistler to provide console interaction handling over the network (Kistler, abstract)

28. Claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boucher as applied to claim 1 above, and further in view of Microsoft (Winsock Direct and Protocol Offload on SANs, 03/03/2001).

29. For claim 14, Boucher does not disclose the unified driver is coupled to a software TCP processor and to a socket service switch, wherein the software TCP processor is coupled to the socket service switch

However, Microsoft discloses the unified driver is coupled to a software TCP processor and to a socket service switch, wherein the software TCP processor is coupled to the socket service switch (Microsoft, fig. 1, a socket switch between a TCP/IP socket provider and a SAN provider), and wherein the socket service switch is coupled to a socket service (Microsoft, fig. 1, switch coupled to socket application).

Therefore, it would have been obvious for one skilled in the art at the time of the invention to combine the teachings of Boucher and Microsoft to provide WinSock socket service switch to a TCP/IP-offload-enabled NIC card of Boucher in order to further enhance the card with more functionalities such as RDMA traffic support.

30. For claim 12, Boucher-Microsoft discloses the invention as in claim 14. Boucher-Microsoft further discloses a plurality of services coupled to the unified driver (Microsoft, fig. 1, p. 5 lines 7-8, socket service, RDMA service).

31. For claim 13, Boucher-Microsoft discloses the invention as in claim 14. Boucher-Microsoft further discloses the particular service comprises at least one of a socket service, a SCSI miniport service, an RDMA service and a keyboard and/or video and/or mouse service (Microsoft, fig. 1, p. 5 lines 7-8, socket service, RDMA service).

32. Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boucher, as applied to claim 18 above, and further in view of Official Notice.

33. For claim 21, Boucher does not disclose (c) comprises employing time division multiplexing to determine which of the different types of network traffic access the software services via the single data path.

However, Official Notice is taken that it is well known in the art how to employ time division multiplexing (TDM) to transmit multiple traffics over one channel in different timeslots.

Therefore, it would have been obvious for one skilled in the art at the time of the invention to combine the teachings of Boucher and what is well known in the art to send multiple traffic over one channel using TDM in order to minimize cost of buildings multiple channels unnecessarily.

34. For claim 22, the claim is rejected for the same rationale as in claim 21 (dynamic allocation of resources is allotting equal time for time division multiplexing of traffics).

35. Claims 5-8 and 24-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boucher, as applied to claim 1 above, and further in view of Hayes et al. (US 2003/0046330, hereafter Hayes)

36. For claim 5, Boucher further discloses the processor comprises a layer 2 network interface card (L2 NIC) (fig. 13, MAC controller 402), a transmission control protocol (TCP) processor (fig. 9, TCP processor for offload).

Boucher does not disclose an upper layer protocol (ULP) processor;

However, Hayes discloses an upper layer protocol (ULP) processor (fig. 3, [0017], NIC with an auxiliary processor for offloading iSCSI upper layer traffic)

Therefore, it would have been obvious for one skilled in the art at the time of the invention to combine the teachings of Boucher and Hayes to provide ULP support for a TCP/IP offload NIC card in order to further enhance the card with more functionalities such as iSCSI traffic support over TCP/IP.

37. For claim 6, Boucher-Hayes discloses the invention as in claim 5. Boucher-Hayes further discloses the TCP processor provides layer 3 processing and layer 4 processing (fig. 9, an offload processor provides L3 IP and L4 TCP offload traffic).

38. For claim 7, Boucher-Hayes discloses the invention as in claim 5. Boucher-Hayes further discloses the TCP processor is shared by at least two of TCP offload traffic (same as claim 6), Internet small computer system interface (iSCSI) traffic (Hayes, [0017]) and RDMA traffic.

39. For claim 8, Boucher-Hayes discloses the invention as in claim 5. Boucher-Hayes further discloses the ULP processor provides iSCSI processing (Hayes, [0017], [0018]).

40. For claim 24, Boucher discloses a method for network interfacing, comprising:
(a) handling a plurality of different types of network traffic via a single Ethernet connector (fig. 13, col. 16 lines 6-12, a network line 210 connected to a MAC controller supporting both offload traffic and regular IP traffic);
(b) processing the plurality of different types of network traffic using a layer 2 (L2) processor (fig. 13, L2 MAC controller 402), a layer 3 (L3) processor and a layer 4 (L4) processor (fig. 9 a TCP/IP offload processor that processes L3 and L4 traffics) and
(c) providing a unified data and control path (fig. 13 links between processor and PCI bus interface).

Boucher does not disclose an upper layer protocol (ULP) processor;

However, Hayes discloses an upper layer protocol (ULP) processor (fig. 3, [0017], NIC with an auxiliary processor for offloading iSCSI traffic);

Therefore, it would have been obvious for one skilled in the art at the time of the invention to combine the teachings of Boucher and Hayes to provide ULP support for a TCP/IP offload enabled NIC card in order to further enhance the card with more functionalities such as iSCSI traffic support over TCP/IP.

41. For claim 25, the claim is rejected for the same rationale as in claim 20.

42. For claim 26, Boucher-Hayes discloses the invention as in claim 5. Boucher-Hayes further discloses the L3 processor and the L4 processor are combined into a single TCP processor (fig. 9, TCP offload processor 230 bypasses (L3 IP and L4 TCP) offload traffic to upper layers (application layer...)

43. For claim 27, the claim is rejected for the same rationale as in claim 24.

44. For claim 28, the claim is rejected for the same rationale as in claim 23.

45. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Boucher-Hayes, as applied to claim 5 above, and further in view of Microsoft.

46. For claim 9, Boucher-Hayes discloses the invention as in claim 5. Boucher-Hayes does not disclose the ULP processor provides RDMA processing

However, Microsoft discloses the same (Microsoft, page 5, Remote DMA semantics including RDMA write and read).

Therefore, it would have been obvious for one skilled in the art at the time of the invention to combine the teachings of Boucher-Hayes and Microsoft to provide WinSock socket service switch between RDMA and TCP/IP in order to further enhance the card with more functionalities such as RDMA traffic support.

Conclusion

47. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- Hendel et al. US 7,142,540. Zero-copy receive buffer management.
- Barrall et al. US 2002/0065924. Hardware acceleration of OS.
- Matters et al. US 6,988,150. System area network.
- Muhlestein et al. US 7,194,519. Filers.
- Cheriton et al. US 6,675,200. Protocol independent support of RDMA.
- Boyd et al. US 2004/0010674. Spilt socket stack.
- Karpoff. US 2001/0049740. Multimedia on demand over WAN.
- Li et al. US 2004/0213205. Voice packet switching.

48. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

49. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hieu T. Hoang whose telephone number is 571-270-1253. The examiner can normally be reached on Monday-Thursday, 8 a.m.-5 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bunjob Jaroenchonwanit can be reached on 571-272-3913. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HH/

BUNJOB JAROENCHONWANIT
SUPERVISORY PATENT EXAMINER
9/17/7

HH